

IN THE CLAIMS

What is claimed is:

- 1 **1.** A semiconductor device, comprising:
 - 2 an insulated gate field effect transistor including
 - 3 a first source/drain area of a second conductivity type formed
 - 4 in a semiconductor area of a first conductivity type;
 - 5 a second source/drain area of the second conductivity type
 - 6 formed in the semiconductor area; and
 - 7 a gate electrode formed on a gate insulating film on a channel
 - 8 area disposed between the first source/drain area and the second
 - 9 source/drain area, the gate insulating film includes a first gate
 - 10 insulating film formed on a first channel area portion and a second
 - 11 gate insulating film formed on a second channel area portion wherein
 - 12 a second type impurity concentration distribution in the first
 - 13 source/drain area is different from the second type impurity
 - 14 concentration distribution in the second source/drain area and a
 - 15 thickness of the first gate insulating film is different from a thickness
 - 16 of the second gate insulating film.
- 1 **2.** The semiconductor device according to claim 1, wherein:
 - 2 a first type impurity concentration distribution in the first channel area
 - 3 portion is different from the first type impurity concentration distribution in the

4 second channel area portion.

1 3. The semiconductor device according to claim 1, wherein:

2 the first gate electrode and the second gate electrode are formed in a
3 side wall configuration.

1 4. The semiconductor device according to claim 1, wherein:

2 the first gate electrode and second gate electrode are electrically
3 connected through a third gate electrode.

1 5. The semiconductor device according to claim 1, wherein:

2 an insulating film is formed between the first gate electrode and the
3 second gate electrode.

1 6. The semiconductor device according to claim 1, wherein:

2 the first channel area portion is adjacent to the first source/drain area
3 and the second channel area portion is adjacent to the second source/drain area
4 wherein the second type impurity concentration in the first source/drain area is
5 lower than the second type impurity concentration in the second source/drain
6 area and the first gate insulating film is thicker than the second gate insulating
7 film

1

1 7. The semiconductor device according to claim 1, further including:

2 a capacitor electrically connected to the first source/drain area; and
3 a bit line electrically connected to the second source/drain area
4 wherein the second type impurity concentration in the first source/drain area is
5 lower than the second type impurity concentration in the second source/drain
6 area.

1 8. The semiconductor device according to claim 7, wherein:

2 the second source/drain area provides a common source/drain area for
3 a pair of memory cells.

1 9. A semiconductor device, comprising:

2 an insulated gate field effect transistor including

3 a first source/drain area of a second conductivity type formed
4 in a semiconductor area of a first conductivity type;

5 a second source/drain area of the second conductivity type
6 formed in the semiconductor area; and

7 a gate electrode formed on a gate insulating film on a channel
8 area disposed between the first source/drain area and the second
9 source/drain area, the channel area including a first channel area and a
10 second channel area, wherein

11 a second type impurity concentration distribution in the first
12 source/drain area is different from the second type impurity
13 concentration distribution in the second source/drain area and a first

14 type impurity concentration distribution of the first channel area is
15 different from the first type impurity concentration distribution of the
16 second channel area.

1 **10.** The semiconductor device according to claim 9, wherein:

2 the gate insulating film includes a first gate insulating film formed on
3 the first channel area and a second gate insulating film formed on the second
4 channel area and a thickness of the first gate insulating film is different from a
5 thickness of the second gate insulating film; and

6 the first gate electrode is formed on the first gate insulating film and
7 the second gate electrode is formed on the second gate insulating film.

1 **11.** The semiconductor device of claim 8, wherein:

2 the first gate electrode and the second gate electrode are formed in a
3 side wall configuration.

1 **12.** The semiconductor device of claim 9, wherein:

2 the first gate electrode and second gate electrode are electrically
3 connected through a third gate electrode.

1 **13.** The semiconductor device of claim 9, wherein:

2 an insulating film is formed between the first gate electrode and the
3 second gate electrode.

1 **14.** The semiconductor device of claim 9, further including:

2 the first channel area is adjacent to the first source/drain area and the
3 second channel area is adjacent to the second source/drain area wherein the
4 second type impurity concentration in the first source/drain area is lower than
5 the second type impurity concentration in the second source/drain area and the
6 first type impurity concentration in the first channel area is lower than the first
7 type impurity concentration in the second channel area.

1 **15.** The semiconductor device of claim 9, further including:

2 a capacitor electrically connected to the first source/drain area; and
3 a bit line electrically connected to the second source/drain area
4 wherein the second type impurity concentration in the first source/drain area is
5 lower than the second type impurity concentration in the second source/drain
6 area.

1 **16.** A manufacturing method of a semiconductor device, the semiconductor device
2 including a first source/drain area of a second conductivity type formed in a semiconductor
3 area of a first conductivity type, a second source/drain area of the second conductivity type
4 formed in the semiconductor area, a gate electrode formed on a gate insulating film on a
5 channel area between the first source/drain area and the second source/drain area, the
6 manufacturing method comprising the steps of:

7 forming a first insulating film on the semiconductor area;

8 forming a first mask layer at a predetermined position on the first
9 insulating film;

10 forming the first source/drain area in the semiconductor area with the
11 first mask layer;

12 forming a second mask layer on the first source/drain area;

13 forming a first channel area of the first conductivity type adjacent to
14 the first source/drain area with the second mask layer;

15 forming a first gate electrode on side walls of the second mask layer;

16 forming a second channel area of the first conductivity type at an
17 essentially central portion of the first channel area with the first gate electrode
18 providing a mask;

19 forming a second insulating film on the second channel area, the
20 second insulating film having a different thickness than the first insulating
21 film;

22 forming a second gate electrode over the second insulating film and
23 separated from the first gate electrode by a mediating insulating film;

24 forming the second source/drain area at a substantially central portion
25 of the second channel area with the second gate electrode providing a mask;
26 and

27 forming a third gate electrode providing an electrical connection for
28 the first gate electrode and the second gate electrode.

1 17. The manufacturing method of a semiconductor device according to claim 16,

2 wherein:

3 a second type impurity concentration distribution of the first
4 source/drain area is different than the second type impurity concentration
5 distribution of the second source/drain area.

1 **18.** The manufacturing method of a semiconductor device according to claim 16,

2 wherein:

3 a first type impurity concentration distribution of the first channel area
4 is different from a first type impurity concentration distribution of the second
5 channel area.

1 **19.** The manufacturing method of a semiconductor device according to claim 16, further

2 including the step of:

3 forming a capacitor electrically connected to the first source/drain
4 area.

1 **20.** The manufacturing method of a semiconductor device according to claim 19,

2 wherein:

3 a second type impurity concentration of the first source/drain area is
4 lower than a second type impurity concentration of the second source/drain
5 area.